

WHAT IS CLAIMED IS:

- 5 1. A wireless communications device, comprising:
a wireless transceiver; and
a processor coupled to the wireless transceiver, the processor having a memory
comprising a plurality of fragments and an array configured to control the sequence of
memory fragments from which data is read.
- 10 2. The wireless communications device of claim 1 wherein the processor further
comprises a second array configured to indicate a status of each of the memory fragments.
- 15 3. The wireless communications device of claim 2 wherein the status indicated by
the second array for each of the memory fragments comprises a bit to indicate whether its
respective memory fragment is empty.
- 20 4. The wireless communications device of claim 1 wherein the processor further
comprises a read pointer configured to indicate the memory fragment from which the data is
being read.
- 25 5. The wireless communications device of claim 1 wherein each of the memory
fragments comprises 64 bytes.
6. The wireless communications device of claim 1 wherein the memory
fragments comprises 128 memory fragments.
- 30 7. The wireless communications device of claim 6 wherein the array comprises a
128 element array.
8. A processor comprising a memory having a plurality of fragments and an array
configured to control the sequence of memory fragments from which data is read.
- 35 9. The processor of claim 8 further comprising a second array configured to
indicate a status of each of the memory fragments.

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10. The processor of claim 9 wherein the status indicated by the second array for
each of the memory fragments comprises a bit to indicate whether its respective memory
5 fragment is empty.

11. The processor of claim 8 further comprising a read pointer configured to
indicate the memory fragment from which the data is being read.

10 12. The processor of claim 8 wherein each of the memory fragments comprises 64
bytes.

13. The processor of claim 8 wherein the memory fragments comprises 128
memory fragments.

15 14. The processor of claim 13 wherein the array comprises a 128 element array.

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